Bringing Insight into the Analysis of Relay Life-Test Failures.

S.J.Hobday BEng(Hons)
Senior Design Engineer, Applied Relay Testing Ltd, England

Abstract **- Applied Relay Testing Ltd is a specialist Company that has created a range of advanced test products dedicated to relays and switch device products. The company's products cover a spectrum of test capability including low-level parametric measurement, contact life-testing and high-voltage performance.**

This paper will illustrate some of the features and benefits of the novel technology employed by the contact measurement 'front-end' of our Reflex50 life-test system. The use of digital signal processing has brought unprecedented levels of test speed, customer programmability and post-failure insight to that most challenging of relay measurement - life-testing. As well as describing the technology employed in making the measurements, the paper will show how the end-user can assign exact measurement parameter windows to the contacts and how any failures are 'frozen', permitting the actual failure mechanisms to be investigated after they happen.

I. INTRODUCTION

The design and construction of relay life-test equipment offers serious technical challenges to the designer. The following issues must be considered:

- Life-testing demands a large number of contacts to be tested simultaneously at close to full relay device operating speed.
- The need to isolate failure information and to provide insight into the possible cause and progression of the failure from within this complex technical environment.

Applied Relay Testing Ltd has met these issues with a novel 'front-end' measurement design, based upon advanced Digital Signal Processing (DSP).

II. MEASUREMENT CONCEPT

Life-testing is mainly based around one simple relay test parameter, that of contact resistance (CR). The primary purpose of a life test is to measure CR whilst the relay contact is CLOSED and to confirm that at least 90 or 95% of the contact load voltage exists when the relay contact is OPEN. A 'comparator' test philosophy is normally adopted for confirming that 90/95% of the contact load voltage is present for an OPEN contact. Our measurement approach for a CLOSED contact CR measurement has also been adopted for CLOSED contact measurements. Figure 1 illustrates how CR is generally measured using an analogue-to-digital converter (ADC) technique:

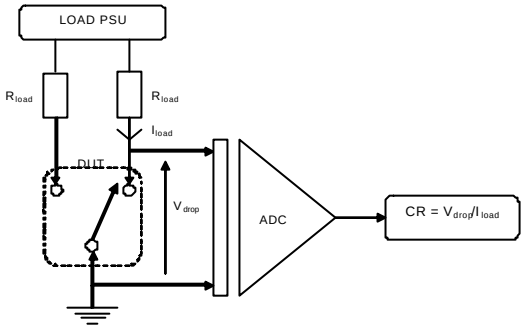

Figure 1 : Basic CR Measurement Technique

The control method used in conjunction with the ADC is design dependant and the ADC can be typically be controlled using the following main method types:

A) Single ADC Measurements
B) Sampling ADC Measurements.

A. Single ADC Measurements

Traditionally, 'in-house' life-testing often harnesses an ADC using a single measurement methodology. Figure 2 illustrates the principles behind this single measurement approach.

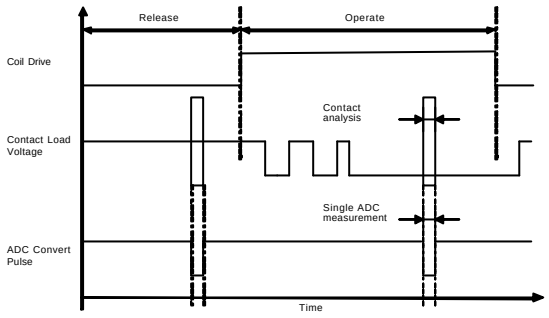

Figure 2: Single ADC Measurement Timing Diagram

Single measurement methods are very simplistic as they only require the ADC to make measurements once or twice per relay cycle. The user specifies the point in time that the ADC performs a measurement. The infrequent trigger rate of the ADC reduces the requirement for a high ADC bandwidth, thus reducing the cost of the measurement process. The cost and speed of testing is normally traded off against measurement precision. Single measurement approaches are less precise as they have limited 'noise immunity' but the overwhelming drawback to this approach is the lack of contact knowledge gained from each measurement. The measurement time is so small on each relay cycle that the collated data is simply a single CR or open contact load voltage, preventing the user from having insight into actual contact activity.

B. Sampling ADC Measurements

Figure 3 illustrates the principles behind a sampling ADC approach.

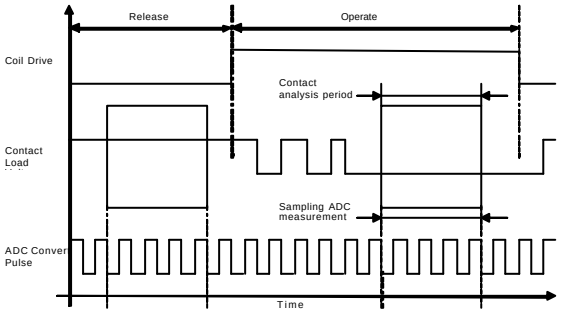

Figure 3: Sampling ADC Measurement Timing Diagram

The sampling ADC measurement approach is naturally more complex since the ADC is being continuously sampled throughout the entire relay contact cycle. The rate at which the ADC is sampled can be made to be a user programmable parameter, thus creating a variable bandwidth measurement unit. Continuous sampling allows multiple ADC measurements to be performed per relay cycle, hence enhancing the user's ability to build a graphical representation of contact activity.

III. OUR GOALS

We set out to design a contact measurement system that would meet the following life-test goals:

A) To provide the user with a greater insight into contact activity.
B) To allow life-test parameters to be input using our graphical user interface approach of defining a programmable measurement window.
C) To gain greater device switching speeds of up to 1 KHz over a variety of load types.

To give the user more insight into contact activity, the measurement unit uses the ADC sampling technique which automatically allows us to obtain multiple measurements throughout a single contact cycle. The measurements obtained are used to formulate a graphical representation of the contact activity, hence giving the user a greater insight into the behaviour of the contact during the life-test sequence.

To provide a graphical 'input' of life-test parameters, we defined a set of programmable values as shown in Figure 4 which shows the programmable measurement window.

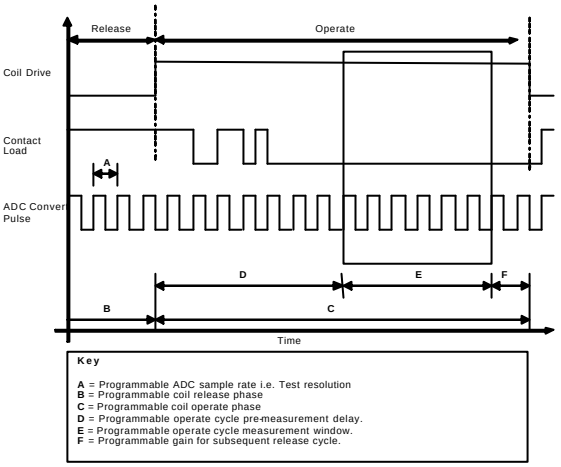

Figure 4 : Fully Programmable Measurement Window

The flexibility of the programmable window approach offers users the ability to generate test sequences using a graphical input engine, automatically giving the user a greater understanding of how their life-test is actually functioning.

Achieving a high relay cycle rate during life-test is not easy. With today's Windows operating systems, it is becoming increasingly common to have 'time stolen' from applications. The apparent 'stealing of time' is a result of an increased number of Windows background tasks, such as networking and printing protocols. This can cause problems with time critical software solutions. This problem can be prevented by

transferring time critical functions into hardware. Life-test applications require the mathematical and computational power of very fast processors, it therefore seems logical for the life-test measurement 'front end' to incorporate a dedicated processor device into the design. With processing power now embodied within the life-test hardware, the main processor control is only required for a Windows environment data display engine.

The computational power of a self sufficient processing unit within the life-test hardware allows us achieve device switching speeds of over 1 KHz even with a variety of loads types. Combining the ADC sampling techniques and mass data storage enables us to offer the end user an enhanced failure analysis approach to life-testing. Text-style failure reports can now be replaced with graphical representation and data logging. Let's now look at how this measurement concept is actually implemented.

IV. MEASUREMENT IMPLEMENTATION

The past few years have seen technological advances in areas such as processors and complex programmable logic devices (CPLD). This has allowed designers to overcome bandwidth limitations without compromise. Our life test measurement 'front end' amalgamates the high speed processing power of a DSP with the re-programmability of a CPLD. Figure 5 identifies the main building blocks of the life-test measurement front end.

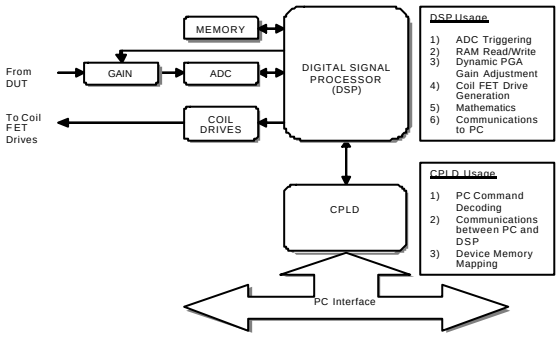

Figure 5: Life-test Measurement Block Diagram

The life-test system architecture is based around interfacing to a standard PC. The PC is used to activate and terminate a life-test sequence, collate life-test data for reporting purposes and indicate useful life-test parameters. Once a life-test has been initiated by the PC, the DSP core sits in a controlled loop performing dedicated life-test requirements. Interfacing the control PC and the life-test measurement hardware is achieved using a CPLD device. The CPLD is used to grant the PC access to specific hardware resources by performing simple PC command decoding procedures. The CPLD grants the PC direct access to the DSP core via a dedicated high speed serial communications port. The DSP expansion bus is directly interfaced to the CPLD, enabling external devices such as memory, ADC's, programmable gain amplifiers and registers to be memory mapped onto the DSP device. This is an essential part of the hardware architecture as it allows the DSP's already powerful architecture to be enhanced further.

The 32-bit floating point DSP is being used purely as a high speed processing unit rather than a digital signal processor. The DSP sits in a controlled loop performing a sequence of hard coded life-test procedures that have been implemented using assembler language, thus allowing tighter control over the DSP code execution and program memory allocation. The DSP has total control over triggering the ADC sampling, reading and writing to memory, dynamic hardware gain changes and the generation of coil drive signals.

V. HOW THE MEASUREMENT FRONT END WORKS

At the start of a life-test, the control PC configures the system from the user specific life-test parameters. Figure 6 identifies the main parameters that the user can program and how they relate to life-testing.

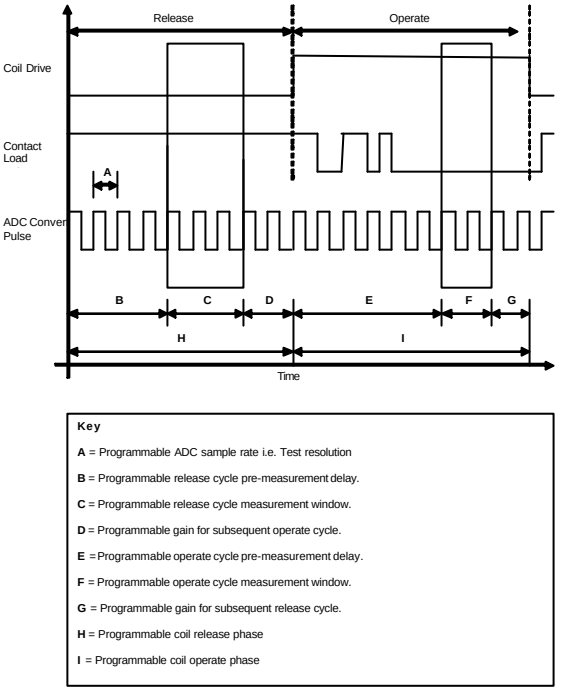

Figure 6 : Life-test Programmable Parameters

The life-test parameters shown in figure 6 are passed to the DSP via a serial communications protocol. The DSP control loop pre-loads these parameters into internal control registers and the PC starts the life-test sequence by writing a start command to the DSP. The initial task of the DSP is to generate an ADC convert pulse that is used to continuously cause the ADC to make a single sample measurement. The frequency of the convert pulse corresponds to the user programmed test resolution. A general purpose timer within the DSP toggles an output at the required convert pulse frequency. The DSP timer generates a timer interrupt after every period of the ADC convert pulse, which is used by the DSP to formulate an event

counter. The event counter is used to sequence when events should commence and terminate i.e. when a pre-measurement delay is complete or when a measurement window is about to start.

The voltage sampled at the ADC input originates from the relay contact under test. A current is passed through the contact under test, creating a potential difference across the contact. The magnitude of this current flowing will be a function of the load type and power supply applied to the contact. The potential difference measured is generally of a small magnitude hence the voltage is passed through a programmable gain amplifier stage to condition the signal into a more manageable level. The gain stage is dynamically modified by the DSP in relation to the contact cycle being tested. The OPEN contact gain is set at the end of the CLOSED contact measurement window and vice-versa. This architecture allows the same measurement technique to be adopted for both OPEN and CLOSED contact measurements.

Every ADC sample is read by the DSP and written to a 64k x 32-bit data storage memory segregated into two banks as shown in figure 7.

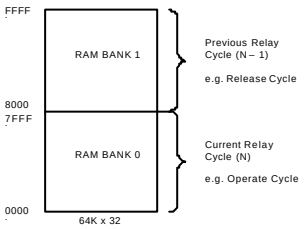

Figure 7 : System Memory Arrangement

This data memory is split into two RAM banks, 0 & 1 respectively. RAM bank 0 always stores the ADC samples for the current relay contact cycle, and RAM bank 1 stores the ADC samples from the previous contact cycle. The shifting of data between RAM banks is performed by the DSP whenever a change in coil drive state is detected. This memory arrangement permits the life-test software to leisurely read system memory and construct graphical representations of contact activity. The life-test software only reads from RAM bank 1, eliminating the risk of corrupting the current contact cycle analysis. The user has access to 32K of data memory purely for contact cycle capturing.

When the event counter signals that the measurement window for a contact cycle is complete, the ADC samples taken within the user defined measurement window are read from memory. All read values are accumulated and averaged to formulate an accurate CLOSED contact or OPEN contact measurement. The DSP uses these calculations to determine whether a life-test failure has occurred. The failure limits for both OPEN and CLOSED contact cycles are specified by the user prior to the life-test sequence commencing. In the event of a life-test failure, the DSP and relay are halted at the end of the current relay cycle. This ensures that the relay will not change state, allowing the system operator to investigate why the failure has occurred. A life-test failure is communicated back to the control PC using the hardware arrangement detailed in figure 8.

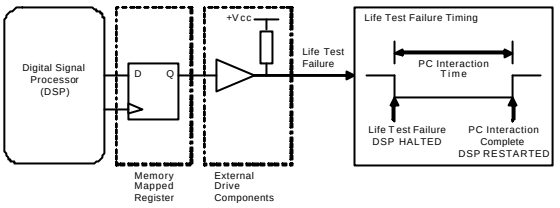

Figure 8: Life-test Failure Indicator

If the control PC detects that the life-test hardware has halted, a status register is read back from the DSP. The information held within the status register is relayed back to the user, identifying exactly why the testing has been halted. Once the user has determined why the failure occurred, the control PC re-initialises the life-test system and the life-test sequence can re-commence.

The benefit of this measurement architecture over traditional approaches is that the PC does NOT dictate the maximum cycle rate of the relay. The advantage is obtained as a result of designing a measurement unit that is purely interrupt driven. The measurement unit functions using two interrupts, these being:

A) Timer Interrupt - Generated with every ADC convert pulse.
B) Serial Port Interrupt - Generated by the communications protocol between the DSP and PC.

As the ADC is continuously being triggered during a life-test sequence, the majority of real time will be spent executing the timer interrupt service routine as opposed to the communications service routine. This means that the DSP will only communicate with the PC when a timer interrupt is inactive, hence preventing time critical life-test functions having ‘time stolen’ from them. This architecture allows us to generate variable relay switching speeds in excess of 1 KHz without degradation in measurement performance.

VI. PRACTICAL RESULTS

A typical life-test overview plot is shown in Figure 9 and shows the minimum and maximum closed device contact resistance by interval.

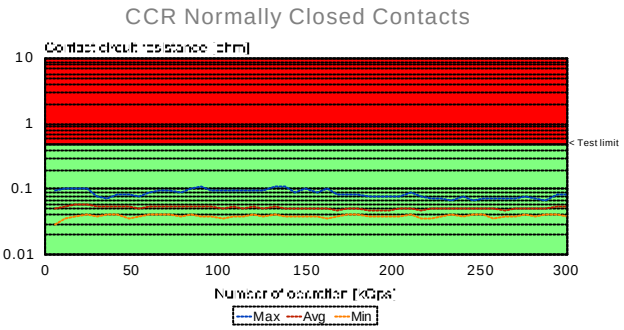

Figure 9 : Standard Closed Contact Life-Test Report

This style of reporting is ideal for identifying the stability of a relay contact but does not show actual contact closure detail, making it hard to assess the actual cause of a failure. Our measurement front-end bridges the gap between this information and more detailed failure analysis, providing contact activity information as shown in figure 10 which shows the contact closure on one life-test switching cycle for a good contact.

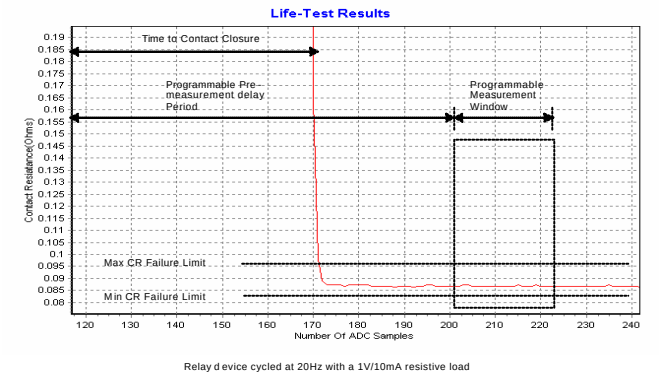

Figure 10 : Reflex50 life-test results - No life-test failures detected

As can be seen, the graphical capability of the Reflex50 gives the user a very clear and precise picture of when the CR measurement occurs for each contact cycle together with much other 'subtle' information such as the cleanliness of the switching (the shape of the closure 'knee') and any slope on the closed contact resistance. The average of all the CR values within the measurement window is still used to provide the CR result for comparison with a failure limit but the additional graphical information is always captured.

As a result, the Reflex50 life-test analysis architecture 'stands out from the crowd' when a life-test failure occurs. The graph shown in figure 11 illustrates the life-test results obtained by the Reflex50 for a relay device that fails the maximum CR limit and therefore would halt a life-test. This failure might occur as a result of the relay closure time degrading over the life-test period (due to mechanical wear for example). Without having our graphical capture representation, the user would be unaware of this mechanism taking place.

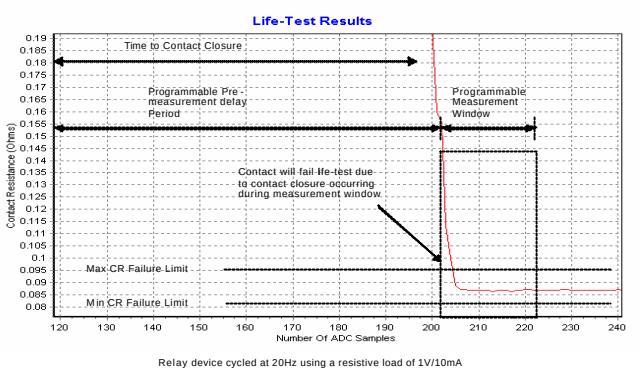

Figure 11 : Reflex50 life-test results – life-test failure detected

The user is now able to clearly identify when life-test failures occur. Traditional life-test systems would possibly be able to detect the CR failures within the measurement window only, leaving the user unaware of the failures that may have occurred prior or after the specified test window. The Reflex50 architecture provides users with more thorough and comprehensive life-test capability.

VII. CONCLUSION

This paper has shown that by employing new technology such as digital signal processors and programmable logic devices has revolutionised life-test measurements, offering users the ability to explore and analyse relay contacts with ease and precision. Graphical user interfaces are now taking over from text-based approaches for both test programming and failure analysis.

To summarise, this new life-test measurement 'front-end' offers the end-user the following benefits:

- A graphical approach to generating test programs.
- Variable relay switching speeds of up to 1 KHz can be achieved.
- Multiple device testing.
- Contact activity monitoring.
- Enhanced failure analysis techniques.
- A flexible system architecture for future enhancements.

VIII. ACKNOWLEDGEMENT.

Applied Relay Testing Ltd thanks the following companies for their support: Teledyne Relays (CA, USA), Axicom AG (Switzerland), Siemens EC (Berlin, Germany), Pickering Electronics (UK).

IX. REFERENCES.

[1] B.J.Frost "A New Relay Test Architecture Brings Low-Cost Parametric Testing and Sophisticated Life-Testing

Together" *Proc. of the 48th relay conference, NARM, April 2000*